because it provides the small form factor to satisfy multifunctional device requirements along with improved signal propagation for optimum performance. New products designed in the front end for WLP applications are smaller than their wirebond counterparts. Overall, WLP enables the next generation of portable electronics at a lower cost.

The mechanical shock resulted from mishandling during

have been developed to satisfy the requirements in package design analysis [10].Various advanced drop test modeling techniques have been developed for various applications, consisting of analysis type (dynamic vs. static), loading method (free-fall vs. input-G), and solver algorithm (explicit vs. implicit). In the so-called Input-G method, the drop table, fixture, contact surface, and friction of guiding rods in drop test setup are not needed to simulate, but their complex effects

a critical solder ball. Since the failure is often at the intermetallic layer or between intermetallic layers [10], a 10 μm intermetallic layer with two layers of mesh is modeled at solder/copper post interface. The material properties used for the local and global finite element models are listed in Table

4. Dynamic Responses of Individual Components on JEDEC Board

Figure 12 shows the maximum peel stresses developed in all components of a quarter test board under impact. Figure 13 shows the peel stress time history plot for all components. It is

calculated at U1 and U8 for both packages. Figure 20 shows the plot for the maximum peel stress for two packages with and without underfill. There is a significant reduction (more than 70%) in the solder joint stress in the presence of underfill. It is apparent that the board strain is not able to capture such an effect. Additional investigations have been conducted on the board strain at locations right beaneth the solder balls. Board strain at these locations indeed capture the trend in solder joint stress but the strain reduction is shwon to be much less than stress reduction.

Figure 20 Maximum Peeling Stress Comparison with and without Underfill at U1

6. Improved JEDEC Board Design

It is known from the earlier investigations that WLP components, which are placed near the mounting holes on JEDEC test board, experience the highest level of stresses in solder joints, therefore, would fail first during drop test. Such observations have not been found in BGA packages. It is important to note that this failure is due to the local bending effect applied due to the mounting hole constraints. In other words, the corner components failures are not caused by the intrinsic factors of WLP package design. In the following discussion, some modifications to existing JEDEC board are made and the new results will shed light to the failure mechanisms of corner components.

According to the current JEDEC board design specification, the mounting hole center is set with a distance of 5mmx5mm from the package corner, regardless of package sizes. In this study, a modified board design is made, which extends the whole board dimension by 4mm × 4mm in length and width directions, such that the mounting hole center will be moved further away from the package corner by an additional 2mmx2mm. The distance between the mounting hole to package corner is 7mmx7mm for the modified board. Figure 21 shows the modified board design. All other geometries remain same.

A 3mm×3mm chip size model is used for both boards. Figure 22 shows the board strain at package corner of component U1 for the two models. It is noted from the figure that board strain decreases significantly for the modified board at U1.

Figure 23 shows the stress time history for standard board and modified board for component U1. It is noted from this figure that there is a significant decrease in stress value for the modified board at component U1.

Figure 24 shows the maximum peel stress in solder balls for all components with standard and modified board designs. There is a significant decrease (more than 30%) in the stress value for modified board at U1, while stresses in other components have trivial changes. Therefore, it is evident from this observation that mounting holes have significant effect on the performance of components nearest to them. This suggests that the failure of components located near mounting cannot

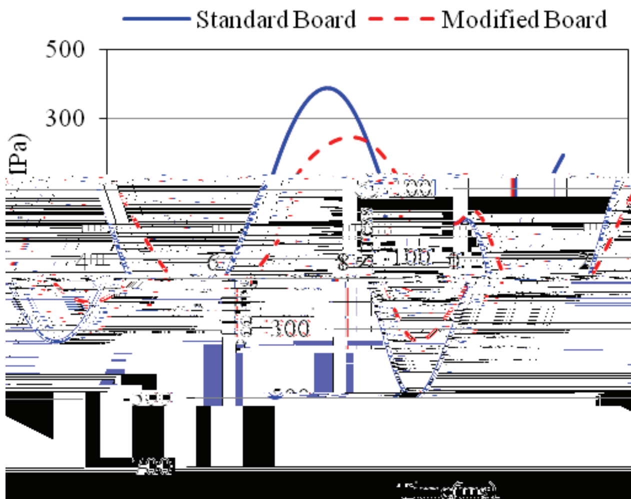

Figure 23 Stress Time History Comparison of Standard JEDEC Board and Modified Board at U1

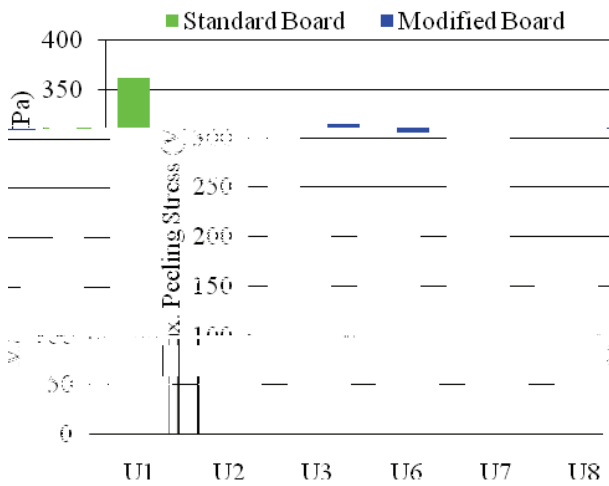

Figure 24 Maximum Peeling Stress Comparison of Standard JEDEC Board and Modified Board

Conclusions

The finite element modeling of dynamic behaviors of wafer level packages under impact loading has been performed. The JEDEC/ JESD22-B111drop test board with Cu post WLP packages were modeled. This paper presented a